Scan-during-sustain method for driving a high resolution AC plasma display panel

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A new method for driving a high resolution AC plasma display panel (PDP) is proposed. The proposed scan-during-sustain (SDS) method is based on the selective erase method for driving an AC PDP, and can drive an SXGA-class (1280 × 1024 pixels) AC PDP without physically dividing the panel electrodes. To overcome the problem of an unacceptably long scan time, the row electrodes of the AC PDP are grouped into eight blocks, with one or two blocks being addressed while the others are sustaining previous states. In each block, the grey levels are implemented using the address-display-period-separation (ADS) method. The scan pulses for the blocks being addressed are applied concurrently with the sustain pulses in the other blocks. An SXGA drive circuit adopting the proposed method has been built and tested on a 40 inch VGA (640 × 480 pixels) AC PDP. Experimental results show that the proposed method can drive 256 grey-level SXGA PDPs with a sufficient sustain margin.

1. Introduction

An AC plasma display panel (AC PDP) is a flat panel display device with the advantage of creating a large, thin, wide viewing angle and a high resolution display screen (Sethi 1998, Voronov and Dedov 1999). The AC PDP displays colours by exciting fluorescent layers with the vacuum ultraviolet (VUV) light emitted from electrically stimulated gas. A typical cell structure and electrode arrangement of an AC PDP with three electrodes is shown in figure 1. The cell consists of two glass plates, two row (scan and common) electrodes, one column (data) electrode, a dielectric/MgO layer and a phosphor layer. The two parallel row electrodes are located between the front glass and the dielectric layer, and the column electrodes are located between the rear glass and the phosphor layer. The row electrodes are orthogonal to the column electrodes and form a matrix pattern. For SXGA-class (1280 × 1024 pixels) full colour AC PDPs, 1024 pairs of row electrodes and 3840 column electrodes are required.

The operation of the AC PDP consists of three basic sequences: address, sustain, and erase operations of PDP cells (Pleshko 1979). During the address operation, a discharge is induced in the cell gap when the externally applied voltage between the scan and data electrodes exceeds the firing voltage. Ions and electrons are generated by the discharge, drift to the dielectric wall, and charge it. The electric charges at the wall (wall charges) cancel the external electric field and the discharge is extinguished. The wall charges supply the memory function for the AC PDP. During the sustain
operation, sustain pulses are applied alternately to the scan and common electrodes. Because the amplitude of the sustain pulse is smaller than the firing voltage, the sustain pulse alone does not induce any discharges. The wall charges help to sustain the discharge for the cells that have been subjected to a previous discharge. The erase operation is accomplished by a weak discharge between the scan and common electrodes. The erase discharge does not produce enough wall charges to induce subsequent sustain discharges. Visible light is emitted when the VUV emitted by the gas discharge excites the fluorescent phosphor layer. The amount of light emission per single sustain discharge is constant, and the grey levels for picture display are implemented by varying the number of sustain pulses.

The most popular method for implementing grey levels in the AC PDP is the sub-field method (Michel 1989, Yoshikawa et al. 1992, Shinoda 1998). The sub-field method uses \( N \)-bit digital video signals and the grey level of each pixel is represented by a polynomial of the form

\[
a_{N-1}2^{N-1} + a_{N-2}2^{N-2} + \cdots + a_12^1 + a_02^0
\]

where the coefficients \( a_i \), \( i = 0, 1, \ldots, N - 1 \), are 0 or 1 and compose digital picture data for each pixel. By collecting the coefficients for each pixel having the same weight, the digital picture data of an image is decomposed into \( N \) sub-field images, \( SF_{N-1}, SF_{N-2}, \ldots, SF_0 \). The most significant bit (MSB) sub-field image \( SF_{N-1} \) consists of data for \( a_{N-1} \), and the least significant bit (LSB) sub-field image \( SF_0 \) consists of data for \( a_0 \). When the sustain period for the \( i \)th sub-field is proportional to \( 2^i \), the

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**Figure 1.** A typical cell structure and electrode arrangement of a three-electrode AC PDP.
amount of light emission is proportional to $2^i$. The video image is recovered by successively displaying the sub-field images.

Two general methods for addressing picture data to the AC PDP are the selective write (Sano 1994, Shinoda et al. 1996) and the selective erase (Hirakawa et al. 1998, Song et al. 1998) methods. Before addressing the data, all cells are turned off by an erase discharge for the selective write method, whereas they are turned on by a write discharge for the selective erase method. Then the picture data are addressed by selectively writing or erasing the cells. The selective write method can achieve a better contrast ratio than the selective erase method because no additional write discharge is required. However, in general, the selective write method requires a longer address period than the selective erase method because the write operation requires a longer pulse than the erase operation.

At present, most PDPs use the selective write method and the address-display-period-separation (ADS) method (Shinoda et al. 1996). In the ADS method, the address period is separated from the sustain period. For high resolution AC PDPs, the required address time for the ADS selective write method becomes too long to be practical. For example, if we assume that the width of the write pulse is 2$\mu$s, the required address period for an SXGA (1280 $\times$ 1024 pixels) AC PDP with 256 grey levels and 60 Hz frame frequency is 16.38 ms ($2\mu$s $\times$ 8 sub-fields $\times$ 1024 rows). Consequently, the available sustain period is only 0.32 ms (one field time of 16.7 ms – 16.38 ms) which is insufficient to display a high quality image. To overcome this problem in the selective write method, the data electrodes for high resolution AC PDPs are divided physically into top and bottom parts, and each part is addressed separately (Uchidoi et al. 1996). Physically dividing the data electrodes requires additional drive circuits and increases the production cost.

Compared with the ADS selective write method, the ADS selective erase method requires a smaller address period because the erase pulse is shorter than the write pulse. When the width of the erase pulse for addressing data is 1.2$\mu$s, the required address period for an SXGA AC PDP with 256 grey levels and 60 Hz frame frequency is 9.83 ms, resulting in an available sustain period of 6.84 ms. This sustain period allows us to drive an SXGA PDP without dividing the data electrodes. However, the achievable brightness is limited because the available sustain period is only 41% of one field time. The available sustain period can be increased further if it is possible to apply the address pulses concurrently with the sustain pulses.

In this paper, we propose a new method for driving a high resolution AC PDP without physically dividing the data electrodes. This scan-during-sustain (SDS) method is based on the selective erase method to reduce the time required for data addressing. The row electrodes of the AC PDP are grouped into several blocks with two blocks (scan blocks) being addressed while the others (sustain blocks) are sustaining previous states. In each block, the grey levels are implemented using the ADS method. To maximize the available sustain period, the scan pulses for the scan blocks are applied concurrently with the sustain pulses in the sustain blocks. The operating principles of the SDS method are explained in §2. Experimental results are given in §3, and conclusions are drawn in §4.

2. Scan-during-sustain method

For a cell of a three-electrode AC PDP, shown in figure 1, we assume that a positive sustain pulse of $\sim 9\mu$s duration is applied to the common electrode while the
scan electrode is grounded. If the cell is turned on by a previous write or sustain discharge, a sustain discharge occurs between the common and scan electrodes. This sustain discharge is extinguished in several hundred nanoseconds after formation of adequate wall charges. Subsequent concurrent application of sustain and data pulses of positive voltage has little effect on wall charges provided that the amplitude of the data pulse does not exceed the firing voltage between the data and row electrodes. Consequently, normal subsequent discharges can be maintained. The proposed scan-during-sustain (SDS) method utilizes this fact.

2.1. Condition for stable sustain discharges

We adopt the selective erase method to implement the SDS method, and assume that the polarities of scan, data and sustain pulses are negative, positive, and positive, respectively. Because the selective erase method is used, all cells to be scanned are turned on before data are addressed. Subsequently, a negative scan pulse and a positive data pulse induce a weak erase discharge. To prevent unwanted discharges by data pulses in a sustaining cell, the amplitude of the data pulse should be limited.

For a sustaining cell, the sustain pulses of voltage $V_s$ are applied to the scan (S) and common (C) electrodes alternately. The data (D) electrode is driven by data pulses.

![Figure 2. Waveforms and wall charge states of a sustaining cell which has been turned on previously.](image-url)
New method for driving a plasma display panel

pulses for the cells to be scanned. Because the sustaining cell shares the D electrode with other cells on the same column, the data pulses are also applied to the sustaining cell. The data pulse, which changes its state according to the picture data, affects the intensity of the sustain discharge at the leading edge of the sustain pulse, resulting in a reduced sustain margin. To avoid this problem, it is necessary to apply a blank pulse to D at the leading edge of the sustain pulse, as shown in figure 2. In figure 2, a blank pulse of width $T_r$ and data pulses of width $T_d$ are applied to D, while a sustain pulse is applied to C. The voltages of the data, sustain and blank pulses are assumed to be $V_d$, $V_s$ and $V_d$, respectively. The four possible wall charge states of a sustaining cell, which has been turned on previously, are also shown in figure 2. Because the cell was subjected to a glow discharge driven by a sustain pulse applied to S, while C was at 0 V and D was at $V_d$, the initial wall voltages are

$$V_{sd}^W = -(V_s - V_d - V_{sd}^p), \quad V_{sc}^W = -(V_s - V_{sc}^p), \quad V_{dc}^W = -(V_d - V_{dc}^p)$$

Here, $V_{sd}^W$, $V_{sc}^W$ and $V_{dc}^W$ are the wall voltages of S with respect to D, S with respect to C, and D with respect to C, respectively. The positive voltages $V_{sd}^p$, $V_{sc}^p$ and $V_{dc}^p$ are the voltages for plasma quenching between the corresponding electrodes. The gap voltages, which are the voltage differences in the gap between electrodes, are close to a sum of the corresponding wall and externally applied voltages. Consequently, the gap voltages at $t_0$, where all electrodes are at 0 V, are

$$V_{sd}^G = -V_s + V_d + V_{sd}^p, \quad V_{sc}^G = -V_s + V_{sc}^p, \quad V_{dc}^G = -V_d + V_{dc}^p$$

At $t_1$, the voltage of D changes to $V_d$, and the gap voltages change to

$$V_{sd}^G = -V_s + V_{sd}^p, \quad V_{sc}^G = -V_s + V_{sc}^p, \quad V_{dc}^G = V_{dc}^p$$

Because it is assumed that the sustain pulse alone does not induce any discharge, no discharge is induced at this period.

At $t_2$, the voltage of C changes to $V_s$, while S is at 0 V and D is at $V_d$. The gap voltages at $t_2$ become

$$V_{sd}^G = -V_s + V_{sd}^p, \quad V_{sc}^G = -2V_s + V_{sc}^p, \quad V_{dc}^G = -V_s + V_{dc}^p$$

When the gap voltage $|V_{sc}^G|$ is higher than the cell firing voltage $V_f$, i.e.

$$V_s > (V_f + V_{sc}^p)/2 \quad (1)$$
a sustain discharge is induced and the wall voltages change to

$$V_{ds}^W \approx -V_{sd}^W = -(V_d - V_{ds}^p) \quad (2)$$

$$V_{cs}^W \approx -V_{sc}^W = -(V_s - V_{cs}^p) \quad (3)$$

$$V_{cd}^W \approx -V_{dc}^W = -(V_s - V_d - V_{cd}^p) \quad (4)$$

resulting in all gap voltages close to the voltages for plasma quenching, i.e.

$$V_{ds}^G \approx V_{ds}^p = -V_{sd}^p, \quad V_{cs}^G \approx V_{cs}^p = -V_{sc}^p, \quad V_{cd}^G \approx V_{cd}^p = -V_{cd}^p$$

At $t_3$, the voltage of D changes to 0 V, while S is at 0 V and C is at $V_s$. The gap voltages become

$$V_{ds}^G = -V_d + V_{ds}^p, \quad V_{cs}^G = V_{cs}^p, \quad V_{cd}^G = V_d + V_{cd}^p$$
At $t_4$, all electrodes are at 0 V, and the gap voltages become

$$V_{DS}^G = -V_d + V_{DS}^P, \quad V_{CS}^G = -V_s + V_{CS}^P, \quad V_{CD}^G = -V_s + V_d + V_{CD}^P$$

When $V_f > V_s > V_d > 0$, all the gap voltages at any time points are less than the cell firing voltage because all plasma quenching voltages are less than $V_s$, and an unwanted discharge is prevented provided that the width of the blank pulse is long enough to last until the sustain discharge extinguishes.

In the case that the previous blank pulse was too short or the sustain discharge was delayed, the blank pulse has no effect on the wall voltages, and the induced initial wall voltages become

$$V_{SD}^W \approx -V_s + V_{SD}^P, \quad V_{SC}^W \approx -V_s + V_{SC}^P, \quad V_{DC}^W \approx V_{DC}^P$$

With these wall voltages, the gap voltages at $t_1$ are

$$V_{SD}^G = -V_d - V_s + V_{SD}^P, \quad V_{SC}^G = -V_s + V_{SC}^P, \quad V_{DC}^G = V_d + V_{DC}^P$$

To prevent unwanted discharge, the following condition should be satisfied:

$$V_d < V_f - V_s + V_{SD}^P$$

The lower limit of $V_d$ is determined by the condition for proper addressing of data. At $t_2$, the gap voltages become

$$V_{SD}^G \approx -V_d - V_s + V_{SD}^P, \quad V_{SC}^G \approx -2V_s + V_{SC}^P, \quad V_{DC}^G \approx -V_s + V_d + V_{DC}^P$$

When the cell firing voltage $V_f$ is less than $|V_{SC}^G| = 2V_s - V_{SC}^P$, a sustain discharge is induced and the wall voltages change to the wall voltages (2), (3) and (4), resulting in all gap voltages being close to the voltages for plasma quenching. From (1) and (5), we have the conditions of $V_s$ for preventing any unwanted discharges:

$$(V_f + V_{SC}^P)/2 < V_s < V_f - V_d + V_{SD}^P$$

For the cells that were turned off by the previous erase discharge, the wall voltage is zero and the magnitudes of gap voltages are $V_d$, $V_s$ or $V_s - V_d$. Because both $V_d$ and $V_s$ are smaller than $V_f$, the data pulses for addressing the other cells do not induce any unwanted discharges on the erased sustaining cells. Accordingly, the conditions (5) and (6) are the required conditions for stable sustain discharges.

2.2. Scan-during-sustain algorithm

An electrode arrangement of an SXGA colour AC PDP for the SDS method is shown in figure 3. One pixel consists of three sub-pixels emitting red, green and blue lights, respectively, and the number of D electrodes is 3840. D electrodes are connected to external terminals alternately at the top and bottom sides of the panel. The number of the S and C electrode pairs is 1024. The row electrodes are grouped into eight blocks: $B_1$, $B_2$, $B_5$ and $B_7$. Each block has 128 pairs of row electrodes. Each S electrode is driven separately, and C electrodes in the same block are electrically connected and driven together. The odd numbered blocks, $B_1$, $B_3$, $B_5$ and $B_7$, use the left side of panel for S and the other side for C. The even-numbered blocks, $B_2$, $B_4$, $B_6$ and $B_8$, have opposite electrode arrangements. By having these arrangements of electrodes, a single type of drive board can be used for both the left and right sides of the panel.
One field time ($\approx 16.7 \text{ ms}$) for 60 Hz frame frequency is divided into forty-five basic periods of duration $T_b \approx 371 \mu\text{s}$. For each basic period, one or two blocks are scanned and the other blocks are sustained. The waveforms for the scan and sustain blocks are shown in figure 4.

The block-write, stabilize and scan pulses are applied in sequence to the scan blocks, while the sustain pulses are applied to the sustain blocks. The leading edge of the block-write pulse has a step at voltage $V_s$ to reduce the intensity of write discharges. The block-write pulse of voltage $V_{wr}$ is applied simultaneously to all C...
electrodes in the scan blocks. Write discharges are induced between C and S of each cell in the scan blocks. At \( t_3 \), a stabilize pulse of voltage \( V_s \) is applied to all S electrodes in the scan blocks. The stabilize pulse overlaps the block-write pulse to prevent the self-erase phenomenon that occurs at the falling edge of the block-write pulse. At \( t_4 \), the block-write pulse returns to zero and the gap voltage between S and C is \( V_s + V_w \), which induces a stabilize discharge. At \( t_5 \), the stabilize pulse returns to zero and all cells of the scan blocks enter ON states. While the block-write and stabilize pulses are being applied, the voltage of all D electrodes is set to \( V_d \) to protect the phosphor layer, and the voltages of all C and S electrodes in the sustain blocks are 0 V. After \( t_5 \), a scan pulse of voltage \( -V_{sc} \) is applied sequentially to the S electrodes in the scan blocks. The scan pulse is synchronized with the data pulses. The data pulses selectively turn off the cells in the row addressed by the scan pulse. While the scan blocks are being addressed, the sustain blocks are driven by the sustain pulses to maintain the state of cells determined by the previous address operation. To increase noise immunity and to protect the phosphor layer at the leading edges of the sustain pulse, the blank pulses are applied to D electrodes and the scan pulse is not applied to S of the scan blocks.

An arrangement of sub-fields is shown in figure 5. In figure 5, the shaded regions represent the sustain periods. The sloped lines \( \backslash \) and \( / \) represent downward and upward scans, respectively. (During the basic period \( T_b \), the rows in the odd numbered blocks are scanned one at a time in ascending order of row number and those in the even-numbered blocks are scanned in descending order.) For one field period, each block scans all eight sub-fields. The sustain period for the sub-field \( SF_i \) is \( 2^i T_b / 8 \), where \( i = 0, 1, 2, \ldots, 7 \), and grey levels are implemented in each block, using the standard ADS method. However, the scan sequences of sub-fields for

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**Figure 5.** An arrangement of the sub-field for the SDS method.
each block are different, to increase the available sustain time. The following scan sequences of sub-fields are adopted:

\[
\begin{align*}
B_1 \text{ and } B_2: & \ SF_5, SF_6, SF_0, SF_1, SF_2, SF_3, SF_4, SF_7 \\
B_3 \text{ and } B_4: & \ SF_6, SF_7, SF_0, SF_1, SF_2, SF_3, SF_4, SF_5 \\
B_5 \text{ and } B_6: & \ SF_5, SF_4, SF_3, SF_2, SF_1, SF_0, SF_7, SF_6 \\
B_7 \text{ and } B_8: & \ SF_7, SF_4, SF_3, SF_2, SF_1, SF_0, SF_6, SF_5
\end{align*}
\]

The scan sequences of sub-fields for block \( B_j \) are the same as those for block \( B_{j+1} \) except that \( B_{j+1} \) scans after \( B_j \), where \( j = 1, 3, 5 \) and 7. On each of the top (\( B_1 \text{–} B_4 \)) and bottom (\( B_5 \text{–} B_8 \)) half of the screen, the scan periods of \( SF_0, SF_1, SF_2, SF_3 \) and \( SF_4 \) for two blocks are placed at the sustain periods of \( SF_7 \) for the other two blocks. For a given basic period, the number of scan blocks on each half of screen is one at most. The scan pulse alternates between the scan blocks on the top and bottom halves of the screen. While the scan blocks are addressed, the other blocks sustain. With these arrangements of sub-fields and scan sequences, the available sustain period for an SXGA AC PDP with 256 grey levels and 60 Hz frame frequency is \((31 + 7/8)/45 \times 100\% = 70.8\%\) of the one field period. When compared with the available sustain period for the ADS selective erase method, which is 41\% of the one field period, this long available sustain period is possible because the SDS method uses the scan pulses applied concurrently with the sustain pulses.

2.3. Drive circuit

A block diagram of the experimental drive circuit for the SDS method is shown in figure 6. It consists of one input controller, one data driver and two row drivers. The input of the drive circuit is 8-bit RGB digital video signals, which are generated by a digital video signal generator. The input controller consists of a display data converter, a frame memory, a data controller, a scan controller and a pulse-shape controller. The display data converter rearranges RGB video data so that the data

![Figure 6. Block diagram of an experimental drive circuit for the SDS method.](image-url)
are appropriate for driving an AC PDP. The frame memory consists of two memory banks: one bank stores one field of video data from the display data converter, while the other outputs one field of preceding video data to the data driver. The data controller outputs timing signals for the data driver. The scan controller outputs timing signals for the scan driver ICs; this is required to implement the SDS algorithm shown in figure 5. The scan pulses are synchronized with the data pulses. The pulse-shape controller outputs timing signals which are required for the row drivers in making the row drive waveforms, as shown in figure 4.

To convert the input 8-bit RGB video data into a format suitable for the SDS method, the input data for one row of the PDP are rearranged first in the display data converter. Because the column electrodes of the PDP for each pixel assume a colour order of RGB, the rearranged data for 3840 columns also follow the same order. Next, the bits of same weight are collected to form eight sub-field data. The sub-field data are stored in one of the memory banks. After storing data for all 1024 rows, the display data converter outputs the picture data for a row sequentially according to the scan sequences shown in figure 5. The output bus-width is 128 and the clock rate is 27 MHz. These 128-bit serial data are converted into 3840-bit parallel data in the data drive ICs.

The row driver consists of one sustain pulse generator, four scan drivers and four common drivers, as shown in figure 7. The sustain pulse generator supplies sustain pulses to the scan and common drivers. One scan driver consists of a scan pulse generator and two switches, and it outputs the scan and sustain pulses to S electrodes of one scan block consisting of 128 pairs of row electrodes. The switches select the scan or sustain pulses using the timing signals from the pulse-shape controller. One

![Figure 7. Schematic diagram of the row drive circuit.](image)
common driver consists of a block-write pulse generator and two switches, and it outputs the block-write and sustain pulses to C electrodes of one block. The row driver 1 drives S electrodes in the odd numbered blocks and C electrodes in the even-numbered blocks. The row driver 2 drives S electrodes in the even numbered blocks and C electrodes in the odd-numbered blocks.

3. Experimental results

Using the SDS method, a drive circuit for the SXGA AC PDP had been built and 1/4 frame drive experiments were performed on a 40 inch VGA (640 × 480 pixels) AC PDP from LG Electronics Inc. A 1/4 SXGA 256 grey-level picture image generated by the VG-825 pattern generator from Astrodesign Inc. was displayed successfully and is shown in figure 8. Operating conditions were \( V_s = 165 \) V, \( V_{wr} = 330 \) V, \( V_d = 60 \) V and \( V_{sc} = -84 \) V. The pulse widths of the waveforms shown in figure 4 were 10 \( \mu s \) for block-write, 20 \( \mu s \) for stabilize, 1.2 \( \mu s \) for scan, 1.2 \( \mu s \) for data and blank, and 9 \( \mu s \) for sustain pulses. The frequency and duty factor of the sustain pulse were 25 kHz and \( \sim 0.225 \), respectively.

The measured waveforms at the basic period 41 for \( S_{428} \) and \( C_4 \) of block \( B_4 \), which is scanning, and that for \( S_{300} \) and \( C_3 \) of block \( B_3 \), which is sustaining, are shown in figure 9. On block \( B_4 \), the block-write and stabilize pulses follow the sustain pulses for basic period 40. Subsequently, a scan pulse for addressing line 428 follows. The sustain pulses for the basic period 42 are applied after the scan period. On block \( B_3 \), which has been addressed at basic period 40, the sustain pulses for the sub-field \( SF_3 \) are applied alternately to \( S_{300} \) and \( C_3 \) at basic periods 41 and 42.

The measured waveforms for \( S_{429} \) (trace 1), \( S_{428} \) (trace 2), \( C_3 \) (trace 3), and \( D_{640} \) (trace 4) are shown in figure 10. On the data waveform \( D_{640} \), the data for lines 429, 941, 428, 940, 427, 939, 426 and 938 are 0, 0, 1, 0, 0, 0, 0 and 1, respectively. The

![Figure 8](image-url)

Figure 8. A 1/4 SXGA 256 grey-level picture image generated by the SDS method. Operating voltages are \( V_s = 165 \) V, \( V_{wr} = 330 \) V, \( V_d = 60 \) V and \( V_{sc} = -84 \) V. The frequency of the sustain pulse is 25 kHz and pulse widths are 10 \( \mu s \) for block-write, 20 \( \mu s \) for stabilize, 1.2 \( \mu s \) for scan, 1.2 \( \mu s \) for data and blank, and 9 \( \mu s \) for sustain.
blank pulse is inserted between the data for lines 429 and 941. The scan pulse for $S_{428}$ of the scanning block $B_4$ is applied concurrently with the sustain pulse for $C_3$ of the sustaining block $B_3$, as required to implement the SDS method.

To measure the range of sustain voltage for proper write, address and sustain operations, the picture shown in figure 8 was displayed on the PDP while changing the amplitude of the sustain pulse. The colours of the displayed picture were red,
green and blue. For each colour, the picture was examined over the entire panel. The range of sustain voltage for proper operation was determined by measuring the sustain voltage at which either an improper addressing or a noisy picture condition occurs on any part of the panel. The measured minimum and maximum sustain voltages for different block-write, data and scan voltages are shown in figures 11, 12 and 13.

The minimum and maximum sustain voltages versus block-write voltage for $V_d = 60\, \text{V}$ and $V_{sc} = -84\, \text{V}$ are shown in figure 11. The voltage of the block-write pulse is limited to $V_s + 215\, \text{V}$ by the voltage rating of FET switches. The hatched area shows the range of sustain voltage for proper operation. The maximum sustain voltage $V_{s\text{max}}$ is almost constant for the voltage range of $130\, \text{V} < V_{wr} - V_s < 215\, \text{V}$. The minimum sustain voltage $V_{s\text{min}}$ is inversely proportional to $V_{wr} - V_s$ for $130\, \text{V} < V_{wr} - V_s < 155\, \text{V}$, and it is constant for $V_{wr} - V_s > 155\, \text{V}$. Below the minimum sustain voltage, insufficient wall charges are formed by the block-write pulse and the cells cannot maintain ON states by sustain pulses. Above the maximum sustain voltages, the block-write discharge is so intense that the cells cannot be turned off with the scan and data pulses.

The effects of data pulse amplitude on $V_{s\text{min}}$ and $V_{s\text{max}}$ for $V_{wr} - V_s = 165\, \text{V}$ and $V_{sc} = -84\, \text{V}$ are shown in figure 12. The voltage of data pulse is limited to $75\, \text{V}$ from the voltage rating of data driver ICs. The $V_{s\text{min}}$ is almost constant for the voltage range of $46\, \text{V} < V_d < 75\, \text{V}$. The maximum sustain voltage $V_{s\text{max}}$ increases sharply with $V_d$ for $42\, \text{V} < V_d < 46\, \text{V}$, and it is almost constant for $V_d > 50\, \text{V}$. When $V_d$ was less than $42\, \text{V}$, an accurate addressing of data was impossible because the erase discharge was too weak. For $V_s < V_{s\text{min}}$, the sustain discharge is too weak to support stable sustain discharges. For $V_d < 50\, \text{V}$ and $V_s > V_{s\text{max}}$, the sustain voltage induces unwanted sustain discharges due to remaining wall charges after weak

![Graph](image_url)

**Figure 11.** The minimum and maximum allowed sustain voltages versus block-write voltage for $V_d = 60\, \text{V}$ and $V_{sc} = -84\, \text{V}$. 
addressing of erase discharges. For \( V_d > 50 \text{ V} \) and \( V_s > V_{s_{\text{max}}} \), the sustain voltage induces unwanted sustain discharges, regardless of cell conditions, after the address discharge.

The effects of scan pulse amplitude on \( V_{s_{\text{min}}} \) and \( V_{s_{\text{max}}} \) for \( V_{wr} - V_s = 165 \text{ V} \) and \( V_d = 60 \text{ V} \) are shown in figure 13. When \( V_{sc} < -99 \text{ V} \), all cells remain in the ON state because the address discharges are strong enough to maintain this state. Further, all cells remain in the ON state when \( V_{sc} > -74 \text{ V} \), because the address discharges are too weak to turn off the cells. For \(-99 \text{ V} < V_{sc} < -83 \text{ V} \), \( V_{s_{\text{max}}} \) decreases with increasing \( |V_{sc}| \), because a strong erase discharge induces more wall charges and less sustain voltage is required to turn off the discharge. For \(-83 \text{ V} < V_{sc} < -74 \text{ V} \), \( V_{s_{\text{max}}} \) increases with increasing \( |V_{sc}| \), because an incomplete wall charge cancellation by a weak erase discharge results in a wall voltage of opposite polarity and the cell cannot be turned off with a high sustain voltage. For \(-99 \text{ V} < V_{sc} < -87 \text{ V} \), \( V_{s_{\text{min}}} \) is constant because the sustain discharge is too weak to maintain the discharge with \( V_s < 150 \text{ V} \). For \(-87 \text{ V} < V_{sc} < -76 \text{ V} \), \( V_{s_{\text{min}}} \) decreases with increasing \( |V_{sc}| \) because a strong erase discharge induces more wall charges and less sustain voltage is required to turn off the discharge.

The luminance for a 60 Hz, 256 grey-level SXGA and a full white picture was measured at the same drive conditions as those for the measurement of sustain margin. The measured luminance for the SDS method, with sustain pulses of frequency 25 kHz and width 4.5 \( \mu \text{s} \), was 148.5 cd/m\(^2\). For the ADS selective erase method, the available sustain period for the picture is 6.84 ms, as discussed in §1. When we use two sustain pulses for the least significant sub-field \( SF_0 \), the required minimum number of sustain pluses is 510. With 25 kHz sustain pulses, the number of available sustain pulses for the ADS selective method is 342 (\( 2 \times 6.84 \text{ ms} \times 25 \text{ kHz} \)), and it is impossible to display a 60 Hz, 256 grey-level, and SXGA picture. To solve

Figure 12. The minimum and maximum allowed sustain voltages versus data voltage for \( V_{wr} - V_s = 165 \text{ V} \) and \( V_{sc} = -84 \text{ V} \).
this problem, and to compare the luminance of the SDS method with that of the ADS selective erase method, the frequency and width of the sustain pulse were changed to 50 kHz and 4.5μs, respectively, while the other conditions were unchanged. The observed sustain margins for the SDS method with 4.5μs sustain pulses were almost the same as those with 9μs sustain pulses, and a good quality SXGA picture was displayed. The measured luminance was 254 cd/m² for the SDS method and 138.1 cd/m² for the ADS selective erase method, resulting in a luminance ratio of ~1.84. This luminance ratio of the SDS to ADS selective erase methods is a little higher than the theoretically predicted ratio of 70.8/41 = 1.73. The difference originates from the limitations on using the sustain pulses to realise 256 grey levels.

4. Conclusions

A scan-during-sustain method for driving a high resolution AC PDP is proposed. The proposed method can drive an AC PDP of SXGA class without physically dividing the panel electrodes. It uses the selective erase method to overcome the problem of an unacceptably long scan time for SXGA picture data. The row electrodes of the AC PDP are grouped into several blocks, with one or two blocks being addressed while the others are being sustained. The scan pulses for the blocks being addressed are applied concurrently with the sustain pulses in the other blocks. For an SXGA AC PDP with 256 grey levels and 60 Hz frame frequency, the available sustain period with the SDS method is 70.8% of the one field period, while that with the conventional ADS selective erase method is 41%. This long sustain period is possible because the SDS method uses a concurrent application of the scan and sustain pulses.
An SXGA drive circuit adopting the proposed method has been built and tested on a 40 inch VGA (640 × 480 pixels) AC PDP. The experimental results show that the proposed method can drive a 256 grey-level SXGA PDP with a sufficient sustain margin. With 4.5 μs sustain pulses, the full white luminance displayed with the SDS method was 254 cd/m², while that displayed with the ADS selective erase method was 138.1 cd/m². Because the SDS method can have a longer available sustain period than the ADS selective erase method, the measured luminance for the SDS method is 1.84 times higher than that for the ADS selective erase method.

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References


